Series 948x
Digital I/O Boards

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The AVME948x Digital Input/Output Boards provide a means for interfacing various discrete devices to a VMEbus based computer. Interfacing is accomplished via software control of 64 general purpose I/O points which may be individually programmed as inputs or outputs. Additionally, eight of these 64 I/O lines may be configured to generate VMEbus interrupts.

This manual covers two models of Digital I/O Boards. Table 1.1 below lists these model numbers and their major differences.

Table 1.1 Model Numbers

MODEL NO.	INTERFACE POINTS	FRONT PANEL ACCESS	REAR ACCESS
AVME 9480	64 I/O	P3, P4	
AVME 9481	64 I/O		P2

KEY FEATURES OF MODEL AVME948x I/O BOARDS

- **High Channel Count** - Provides up to 64 programmable I/O points (lines) configured as eight 8-bit ports, or four 16-bit ports.
- **Output Readback** - The state of output points can be read.
- **High Sink Capability** - Outputs may sink up to 100mA at voltages up to 30V.
- **Output Protection** - Built in protection diodes for driving inductive loads.
- **Wide Input Range** - Input range of 0 to 30V.
- **Wide Input Hysteresis** - Input hysteresis is included.
- **Adjustable Input Threshold** - Input threshold is adjustable.
- **Termination Panel/Solid-State Relay Interface** - Compatible with industry standard solid-state relays and termination panels, PB16 and PB32.
- **TTL/CMOS** - TTL and CMOS compatible.

- **Optional Termination Panel** - Optional universal termination panel available for use with contact closures, relays, and incandescent lamps.
- **Byte or Word Interchange** - Byte or word data transfers.
- **Built-in ID PROM** - On board identification PROM included.
- **Port 0 Interrupt Handling** - Port 0 may be used for handshaking mode with both flag and interrupt capability.
- **Status Indicators** - Pass/Fail status indicators on front panel.
- **Front or Back I/O Access** - I/O points are accessible through the front panel or out of the back of the card cage.

VMEbus INTERFACE FEATURES

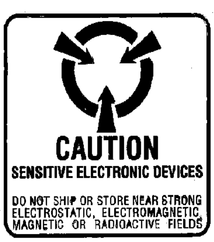
- **Slave Module** - Slave Module A16, D16/D08(E0).
- **Release-On-Register Access Interrupts** - D08(0) RORA type Interrupter.
- **Single/Multiple Input Vectors** - Single or Multiple Interrupt Vectors.
- **Short Addressable** - Responds to short address modifier codes 29H, 2DH (a capital H suffix indicates a hexadecimal number).
- **Low Memory Consumption** - Board occupies 1K bytes of memory space (jumper selectable).
- **ID PROM** - Board Identification PROM installed.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.



This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the electrical specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the board, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

BOARD CONFIGURATION

This Digital I/O Board may be configured in a variety of ways for many different applications. Each possible jumper setting will be discussed in the following sections. The jumper locations are shown in Drawing 4500-981 at the back of this manual.

Default Jumper Configuration

A board is shipped from the factory configured as follows:

- VMEbus Short I/O Address of 0000H.
- Set to respond to both address modifiers 2DH and 29H.
- All of the ports have the reference and pullup resistors connected to +5 Volts.
- Board will assert SYSFAIL* after power-up or reset.

ADDRESS ASSIGNMENT

Jumpers J17 and J19 are used to establish the base address for the 1Kbyte block of memory that the AVME948x will occupy in the short I/O memory map. J17 selects the base address, while J19 selects the address modifier codes. An open jumper corresponds to a logic 0 state for the base address. For the address modifier code, an open jumper selects the Short Supervisory Access (2DH) code and a jumper short will allow the card to recognize both the Short Supervisory and the Short Non-Supervisory Access (29H) codes.

Table 2.1 VMEbus Address Decode Jumper (J17 Pins)

BASE ADDR (HEX)*	A15 (11&12)	A14 (10&9)	A13 (8&7)	A12 (6&5)	A11 (4&3)	A10 (2&1)
0000	OUT	OUT	OUT	OUT	OUT	OUT
0400	OUT	OUT	OUT	OUT	OUT	IN
0800	OUT	OUT	OUT	OUT	IN	OUT
0C00	OUT	OUT	OUT	OUT	IN	IN
1000	OUT	OUT	OUT	IN	OUT	OUT
⋮	⋮	⋮	⋮	⋮	⋮	⋮
EC00	IN	IN	IN	OUT	IN	IN
F000	IN	IN	IN	IN	OUT	OUT
F400	IN	IN	IN	IN	OUT	IN
F800	IN	IN	IN	IN	IN	OUT
FC00	IN	IN	IN	IN	IN	IN

* Consult your host CPU manual for detailed information about addressing the VMEbus short I/O space (A16, 16-bit). In many cases, CPU's utilizing 24-bit addressing will start the 16-bit addressing at FF0000 (Hex), and 32-bit CPU's at FFFF0000 (Hex).

PORT JUMPERS AND OPTIONS

Several jumpers have been included for flexibility in interfacing to external devices. Table 2.2 describes these jumpers and their functions.

Table 2.2 Jumper Descriptions

Jumper	Function	As Shipped
J8	(Ports N+O & N+1 reference voltage). When in place, sets thresholds for input to +1V and +2.2V (TTL) low and high, respectively. Remove J8 to establish reference off card.	Jumper in place
J7	(Ports N+0 & N+1 pullup voltage jumper). When in place, pulls the I/O lines to +5V through the optional pullup networks.	Jumper in place
J6	(Ports N+2 & N+3 reference voltage). When in place, sets thresholds for input to +1V and +2.2V (TTL) low and high, respectively. Remove J6 to establish reference off card.	Jumper in place
J5	(Ports N+2 & N+3 pullup voltage jumper). When in place, pulls the I/O lines to +5V through the optional pullup networks.	Jumper in place
J2	(Ports N+4 & N+5 reference voltage). When in place, sets thresholds for input to +1V and +2.2V (TTL) low and high, respectively. Remove J2 to establish reference off card.	Jumper in place
J1	(Ports N+4 & N+5 pullup voltage jumper). When in place, pulls the I/O lines to +5V through the optional pullup networks	Jumper in place
J4	(Ports N+6 & N+7 reference voltage). When in place, sets thresholds for input to +1V and +2.2V (TTL) low and high, respectively. Remove J4 to establish reference off card.	Jumper in place
J3	(Ports N+6 & N+7 pullup voltage jumper). When in place, pulls the I/O lines to +5V through the optional pullup networks.	Jumper in place
J16	Port N+0 output driver enable	J9-J16 ** are made with a thin trace on the solder side. Cutting jumper will disable the outputs of that group.
J9	Port N+1 output driver enable	
J15	Port N+2 output driver enable	
J10	Port N+3 output driver enable	
J14	Port N+4 output driver enable	
J11	Port N+5 output driver enable	
J13	Port N+6 output driver enable	
J12	Port N+7 output driver enable	
J18	DTACK* Timer Jumper - This jumper is preset at the factory and should not be reprogrammed by the user.	Factory programmed
J20	SYSFAIL* Jumper - This asserts SYSFAIL* after power up or reset.	Jumper in Place

** J9-J16 are used only in cases where it is absolutely necessary to have outputs disabled through the hardware. See Programming Considerations (Section 3) for instruction on software enabling/ disabling of outputs.

Input Threshold Adjustment

Different input thresholds may be established by connecting REF to a voltage other than +5V. When this is done, the input hysteresis still remains at approximately 1.2 volts. The new high and low thresholds are defined by the following equations:

V_{LOW} = (0.448 x REF)- 1.22;
V_{HIGH} = (0.448 x REF) + 0.025;
$2.75 \leq REF \leq 27.5$ Volts

I/O CONNECTIONS

On Model AVME 9481, the 64 I/O points are accessible through a 96-pin DIN 41612 connector labeled P2. I/O adapter card Models 9921-16 or 9921-32 are used to interface between P2 and the ribbon cables (see Drawings 4500-788 & 4500-789). These adapters mount to the back of a VME cage to provide the mating socket for P2. Refer to Table 2.3 and the termination panel connection diagrams 4500-790 and 4500-791.

On Model AVME 9480, two 50-pin ribbon cable connectors on the front panel are used to access the 64 I/O points (P3 and P4). I/O adapter card Models 9920-16 or 9920-32 are used to interface between P3 & P4 and the ribbon cables (see Drawings 4500-786 and 4500-787). Refer to Table 2.3 and the termination panel connection diagrams 4500-785 and 4500-792.

CAUTION: DO NOT PLUG P2 INTO ANY BACKPLANES IN A CARD CAGE!

Table 2.3A: I/O Connectors P2,P3

Functions	P2 Pin #	P3 Pin #
Port N+0, I/O Bit 7	B25	33
Bit 6	B26	35
Bit 5	B27	37
Bit 4	B28	39
Bit 3	B29	41
Bit 2	B30	43
Bit 1	B31	45
Bit 0	B32	47
Port N+1, I/O Bit 7	B17	34
Bit 6	B18	36
Bit 5	B19	38
Bit 4	B20	40
Bit 3	B21	42
Bit 2	B22	44
Bit 1	B23	46
Bit 0	B24	48
+5V	B9	1,49
GND	B13,B14	9,11
GND	B15,B16	13,15
REF Ports 0 & 1	B12	7
Pullup Ports 0 & 1	B11	5
Protect Ports 0 & 1	B10	3
Port N+2, I/O Bit 7	A25	17
Bit 6	A26	19
Bit 5	A27	21
Bit 4	A28	23
Bit 3	A29	25
Bit 2	A30	27
Bit 1	A31	29
Bit 0	A32	31
Port N+3, I/O Bit 7	A17	18
Bit 6	A18	20
Bit 5	A19	22
Bit 4	A20	24
Bit 3	A21	26
Bit 2	A22	28
Bit 1	A23	30
Bit 0	A24	32
+5V	B1	2,50
GND	B5,B6	10,12
GND	B7,B8	14,16
REF Ports 2 & 3	B4	8
Pullup Ports 2 & 3	B3	6
Protect Ports 2 & 3	B2	4

Table 2.3B: I/O Connectors P2 & P4

Functions	P2 Pin #	P4 Pin #
Port N+4, I/O Bit 7	C25	33
Bit 6	C26	35
Bit 5	C27	37
Bit 4	C28	39
Bit 3	C29	41
Bit 2	C30	43
Bit 1	C31	45
Bit 0	C32	47
Port N+5, I/O Bit 7	C17	34
Bit 6	C18	36
Bit 5	C19	38
Bit 4	C20	40
Bit 3	C21	42
Bit 2	C22	44
Bit 1	C23	46
Bit 0	C24	48
+5V	C9	1,49
GND	C15,C16	9,11
GND	C13,C14	13,15
REF PORTS 4 & 5	C12	7
Pullup Ports 4 & 5	C11	5
Protect Ports 4 & 5	C10	3
Port N+6, I/O Bit 7	A8	17
Bit 6	A7	19
Bit 5	A6	21
Bit 4	A5	23
Bit 3	A4	25
Bit 2	A3	27
Bit 1	A2	29
Bit 0	A1	31
Port N+7, I/O Bit 7	A16	18
Bit 6	A15	20
Bit 5	A14	22
Bit 4	A13	24
Bit 3	A12	26
Bit 2	A11	28
Bit 1	A10	30
Bit 0	A9	32
+5V	C1	2,50
GND	C5,C6	10,12
GND	C7,C8	14,16
REF Ports 6 & 7	C4	8
Pullup Ports 6 & 7	C3	6
Protect Ports 6 & 7	C2	4

BACKPLANE REQUIREMENTS

The AVME9480 is electrically and mechanically compatible with the VMEbus Specification. The backplane connection is made through the 96-pin DIN 41612 connector labeled P1. The signals used are listed in Table 2.4.

Table 2.4: Backplane Connector P1

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00		D08
2	D01		D09
3	D02		D10
4	D03	BG 0 IN*	D11
5	D04	BG 0 OUT*	D12
6	D05	BG 1 IN*	D13
7	D06	BG 1 OUT*	D14
8	D07	BG 2 IN*	D15
9	GND	BG 2 OUT*	GND
10	SYSCLK	BG 3 IN*	SYSFAIL*
11	GND	BG 3 OUT*	BERR*
12	DS1*		SYSRESET*
13	DSO*		LWORD*
14	WRITE*		AM5
15	GND		
16	DTACK*	AM0	
17	GND	AM1	
18	AS*	AM2	
19	GND	AM3	
20	IACK*	GND	
21	IACKIN*		
22	IACKOUT*		
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31			
32	+5V	+5V	+5V

USE WITH SOLID-STATE RELAYS

The AVME984X Digital I/O Board may interface with industry standard Solid-State relays and termination panels PB16A, PB32, and their equivalents.

Configuring The AVME948x

On Model AVME948x, the following jumpers or shorting clips should be in place: J1,J2,J3,J4,J5,J6,J7 and J8. Pullup resistor networks R57, R50, R56, R51, R35, R52, R54, and R53 are optional.

Table 2.5 lists the Module Number Bit Positioning for the I/O port registers.

Table 2.5 Module Number Bit Positioning

I/O Port Number	Module Number 7 6 5 4 3 2 1 0	PB16A Connected To
N+0	7 6 5 4 3 2 1 0	P3
N+1	15 14 13 12 11 10 9 8	P3
N+2	7 6 5 4 3 2 1 0	P3
N+3	15 14 13 12 11 10 9 8	P3
N+4	7 6 5 4 3 2 1 0	P4
N+5	15 14 13 12 11 10 9 8	P4
N+6	7 6 5 4 3 2 1 0	P4
N+7	15 14 13 12 11 10 9 8	P4

For bit positions corresponding to output modules, a "1" state will turn the I/O point on and the output latch will draw current. A "0" state will turn the module off. For bit positions corresponding to input modules, a "1" state indicates the presence of a low voltage for the "on" state of the module. A "0" state indicates a high voltage is present.

Configuring The PB16A

If the PB16A is to receive power from the AVME9480, install a jumper at pin 1 or pin 49 of the PB16A termination panel. Install appropriate solid-state relay modules. Then connect the 50-pin ribbon cable between the PB16A and the AVME9480 while observing the pin 1 index mark.

USE WITH OTHER DEVICES

The AVME9480 Digital I/O Board can interface to a variety of discrete devices, such as relays, switches, contact closures, and indicators. The optional termination panel Model 6980-16U can be used to connect field wiring to the digital I/O card. The following guidelines should be followed to insure proper interfacing.

Relays And Other Inductive Loads

When driving relays coils or other inductive loads, the PROTECT line should be tied to the voltage supply of the loads. This puts a suppression diode across each load to limit the voltage spike (reverse emf) generated when an inductive load is switched off quickly. However, since PROTECT is common to all 16 outputs, the supply voltage for all of the loads must be the same. Otherwise, each load must have its own external diode and the pullup resistors should be removed from the digital I/O card. See Drawing 4500-743 for relay driver configurations.

Contact Closures And Switches

When sensing contact closures that already are connected to a voltage source, the pullup resistor networks should be removed. The input voltage should be within the range listed in the specifications. For isolated or grounded contacts, the pullups and the +5 volt supply can be used to establish an input voltage. See Drawing 4500-743 for various input configurations.

3.0 PROGRAMMING INFORMATION

This section provides the specific information necessary to program the Digital I/O Board.

MEMORY MAPS

The memory map for the Industrial Digital I/O board, a non-intelligent I/O architecture, is shown in Table 3.1. The Digital I/O board is addressable on 1Kbyte boundries in the short address space. All Acromag VMEbus non-intelligent slaves have a standard interface configuration which consists of a 32 byte on-board ID PROM and a board status register. The rest of the 1Kbyte address space contains registers or other memory specific to the function of the board. All addresses are in hexadecimal. The letters R and W indicate whether a register may be Read and/or Written to. The areas marked "undefined" in the memory map will read with all bits high (1's). These areas are reserved for future use. For future compatibility, application programs should not use these areas for any reason.

Table 3.1: AVME948x Digital I/O Board Memory Map

Base Addr+ (Hex)	EVEN Byte D15 D08	ODD Byte D07 D00	Base Addr+ (Hex)
00 ↓ 3E	Undefined	R - Module ID PROM	01 ↓ 3F
40 ↓ 7E	Undefined	Undefined	41 ↓ 7F
80	R/W-Interrupt Pending/Clear	R/W - Status/Control	81
82	R - Int. Inputs	R/W-Interrupt Enable	83
84	R/W - Int. Level	R/W-Interrupt Polarity	85
86	Undefined	R/W-Point 0 Vector	87
88	Undefined	R/W-Point 1 Vector	89
8A	Undefined	R/W-Point 2 Vector	8B
8C	Undefined	R/W-Point 3 Vector	8D
8E	Undefined	R/W-Point 4 Vector	8F
90	Undefined	R/W-Point 5 Vector	91
92	Undefined	R/W-Point 6 Vector	93
94	Undefined	R/W-Point 7 Vector	95
96 ↓ FE	Undefined	Undefined	97 ↓ FF
100	R/W -I/O Port 0	R/W -I/O Port 1	101
102	R/W -I/O Port 2	R/W -I/O Port 3	103
104	R/W -I/O Port 4	R/W -I/O Port 5	105
106	R/W- I/O Port 6	R/W -I/O Port 7	107
108 ↓ 3FE	Undefined	Undefined	109 ↓ 3FF

Board Identification ID PROM (Read Only, 01-3F)

The Board Identification PROM occupies the 32 odd bytes beginning at location 01. These bytes contain ASCII character strings that identify various characteristics of the board (See Table 3.2).

Table 3.2: Digital I/O Board Identification (ID) PROM

Hex Offset From Board Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	V	56	All VME Boards Have "VMEID"
03	M	4D	
05	E	45	
07	I	49	
09	D	44	
0B	A	41	Manufacturer ID - "ACR" for Acromag
0D	C	43	
0F	R	52	
11	9	39	Board Model No. Unique for Each Model (4 Char + 3 Trailing Blanks)
13	4	34	
15	8	38	
17	0	30	
19		20	
1B		20	
1D		20	
1F	1	31	Number of Kbytes of Address Space Used. If equal "0", then Address Space is indicated at byte 29H.
21		20	
23		20	
25		20	
27		20	
29 ↓ 3F	Undefined		Reserved

Status/Control Register (Read/Write, 81)

The Status/Control Register reflects and controls functions globally on the card.

MSB 7	6	5	4	3	2	1	LSB 0
RSV	RSV	RSV	SW Rst	Global Int Enable	Global Int Pending	Grn LED	Red LED

The bits of the Status Control Register have the following function:

BIT	NAME	DESCRIPTION
Bit 7		Reserved for future use - equals "0" if read
Bit 6		Reserved for future use - equals "0" if read
Bit 5		Reserved for future use - equals "0" if read
Bit 4	Software Reset (W)	Software Reset (W) - Writing a "1" to this bit causes a software reset. Writing "0" or reading the bit has no effect. A software reset turns all of the ports off, which effectively programs the ports for inputs. The effect of a software reset on the various registers is determined in the discussion of each of the registers. NOTE: If a reset is performed when interrupts are enabled, then in order to completely reset the AVME948x, it is necessary to perform two software resets with a delay of at least 2 microseconds between them. This is to prevent a spurious interrupt being caused by the latency of the actual field output being read back at a later time by the input circuit.
Bit 3	Global Interrupt Enable (R/W)	Global Interrupt Enable (R/W) - writing a "1" to this bit enables interrupts to occur from the AVME9480 card. A "0" prevents interrupts. Reset Condition: Set to "0", all interrupts disabled.
Bit 2	Global Interrupt Pending (R)	Global Interrupt Pending (R) - this bit will be a "1" when there is an interrupt pending from any of the interrupt inputs. This bit will be "0" when there are no interrupts pending. Reset condition: Set to "0", no interrupts pending.
Bit 1	Green LED (R/W)	Green LED (R/W) - when written this bit will control the state of the green LED on the front panel. A "1" will turn it on, a "0" will turn it off. Reading it will reflect its current state. Reset Condition: Set to "0", LED off.
Bit 0	Red LED (R/W)	Red LED (R/W) - when written this bit will control the state of the red LED on the front panel. A 1 will turn it off, a 0 will turn it on. Reading it will reflect its current state. Reset Condition: Will read a "0", LED lit, and SYSFAIL* is set low.

The status register bits 1 and 0, along with the Green and Red LED's, provide the user with a means of keeping track of a card's functionality in the system. Since there is no intelligence on the board, the host computer controls these bits. The following is one possible use of these bits in the status register and the LED's on the front panel.

On power-up, the bits in the status register will read low, with the Green LED OFF, the Red LED ON, and SYSFAIL* LOW. This indicates that the board has failed or that it hasn't been tested yet.

The Status Register Bit 1 reads LOW and Bit 0 reads HIGH. The LED's will both be OFF and SYSFAIL* HIGH. This indicates an inactive board.

The Status Register Bit 1 reads HIGH and Bit 0 reads LOW. The LED's will both be ON and SYSFAIL* LOW. This indicates that the board is undergoing a diagnostic checkout.

The Status Register Bits 1 and 0 read HIGH. The Green LED will be ON with the Red LED OFF and SYSFAIL* HIGH. This indicates that the board is fully functional.

VME Interrupter

The VME Interrupter is made up of a series of registers that control the eight I/O interrupt points and the interrupt mode. Refer to the Interrupter Block Diagram (Drawing 4500-740) and the memory map (Table 3.1) for items referenced in the following discussion.

The VME interrupter on the Digital I/O card is a Release On Register Access (RORA) type interrupter and will return an eight bit vector during the interrupt acknowledge cycle. The RORA type interrupter will release the interrupt request line (IRQx*) after the interrupt has been cleared. The interrupter logic contains a programmable interrupt level accessible through the Interrupt Level Register.

The eight I/O interrupt points are level sensitive and prioritized. Interrupt point 7 has the highest priority and interrupt point 0 has the lowest priority. Each I/O interrupting point may be programmed with its own interrupt vector. Further, each I/O interrupt point may be individually masked and the interrupt polarity selected. Refer to the following paragraphs for further discussion of the interrupt registers.

Interrupt Pending/Clear Register (Read/Write, 80)

The Interrupt Pending Register reflects the status of the eight I/O interrupt points from I/O Port 0. A "1" in a bit position indicates an interrupt is pending for the corresponding point. Each bit is the logical AND of its associated "Interrupt Enable" and "Interrupt Input" bits. Hence, an input that is not enabled will never have its interrupt pending bit set to a "1".

An individual interrupt can be cleared by writing a "1" to its bit position if the input level has been negated. If the input level has not been negated, then the individual point must be masked or the interrupt level must be changed in the "Interrupt Input Polarity Register", and then a 1 written to its bit position in the "Interrupt Pending/Clear Register". This is the only way to clear interrupts from the board. This is known as the "Release on Register Access" (RORA) method as defined in the VME System Architecture.

Interrupt Pending/Clear Register for I/O Port 0 Inputs

MSB 7	6	5	4	3	2	1	LSB 0
Point 7	Point 6	Point 5	Point 4	Point 3	Point 2	Point 1	Point 0

Reset Condition: All interrupts cleared.

Interrupt Inputs Register (Read, 82)

The Interrupt Inputs Register provides the status of the eight I/O interrupt points prior to the point where they are masked by the "Interrupt Enable" register. This allows the level detecting circuitry for some inputs to be used in a polled or non-interrupt mode, while others operate in an interrupt mode. A "1" in a bit position indicates the input went through the transition defined by the "Interrupt Input Polarity Register". A write to the corresponding "Interrupt Clear Register" bit will clear the interrupt input flag if the input level has been negated. If the input level has not been negated, then the interrupt input flag will remain set.

Interrupt Inputs Register for I/O Port 0 Inputs

MSB 7	6	5	4	3	2	1	LSB 0
Point 7	Point 6	Point 5	Point 4	Point 3	Point 2	Point 1	Point 0

Reset Condition: All interrupt inputs cleared unless the interrupt condition is still present.

Interrupt Enable Register (Read/Write, 83)

The Interrupt Enable Register provides a mask bit for each of the eight I/O interrupt points. A "0" in a bit position will prevent the corresponding I/O interrupt point from causing an interrupt. A "1" will allow the input to cause an interrupt (providing the global interrupt enable bit is set).

Interrupt Enable Register for I/O Port 0 Inputs

MSB 7	6	5	4	3	2	1	LSB 0
Point 7	Point 6	Point 5	Point 4	Point 3	Point 2	Point 1	Point 0

Reset Condition: All interrupt points masked.

Interrupt Level Register (Read/Write, 84)

The Interrupt Level Register maintains the interrupt level (1-7) that the board responds with when it issues an interrupt request to the VMEbus.

Reset Condition: Register unaffected.

Interrupt Input Polarity Register (Read/Write, 85)

The Interrupt Input Polarity Register determines the level that will cause an interrupt for each of the eight I/O interrupt points. A "1" in a bit position means that an interrupt will occur when the I/O interrupt point is high. A "0" in a bit position means that an interrupt will occur when the I/O interrupt point is low.

Interrupt Input Polarity Register for I/O Port 0 Inputs

MSB 7	6	5	4	3	2	1	LSB 0
Point 7	Point 6	Point 5	Point 4	Point 3	Point 2	Point 1	Point 0

Reset Condition: All inputs will cause interrupts when I/O Interrupt Point is low.

Interrupt Vector Registers (Read/Write, Odd-Bytes from 86-95)

The Interrupt Vector Registers maintain the interrupt vectors for each of the eight I/O interrupt lines. This allows each I/O interrupt line to be serviced by its own software handler. A single software handler can be used by simply making all of the vectors the same. In this case, the handler will have to determine the interrupting point by examining the "Interrupt Pending Register".

Reset Condition: Registers unaffected.

Digital I/O Port Registers (Read/Write, 100-107)

The I/O Port Registers reflect and/or control the state of the bidirectional I/O points. Points are grouped 8 to a port. To use a point as an input, first write a 0 to it to cause the output driver to go into an OFF (high impedance) state. That lets the point be pulled to a high voltage level by an onboard pull-up resistor. The point may then be driven by an external device. Reading the point will reflect the INVERTED level at the I/O connector. To use a point as an output, write the desired "1" or "0" to the point. If the point is read, it will reflect the state of the output as well.

Note that because inverted logic is used, a high level at the I/O connector is read as a "0" in the Port Registers and a low level is read as a "1". This is consistent with the use of open-collector outputs to drive relays and switches. A logic "1" in the computer produces a low level at the output driver to "pull in" a relay and turn something "ON".

Reset Conditions: All of the I/O points are set to "0" which causes the output drivers to go into an OFF (high impedance) state. The result is that all I/O points are configured as inputs.

INTERRUPT BEHAVOIR

Several interrupt schemes are possible with the board's register architecture. Some of the possibilities are:

- Each point serviced by a separate software interrupt handler routine.
- A single software handler for the entire board.
- A mix of some points causing interrupts, some polled.

Two different interrupt release methods are described in the VME System Architecture. They are Release On Register Access (RORA), and Release On Acknowledge (ROAK). The architecture of this board follows the RORA method. This means that an interrupt request is removed from the bus when the associated interrupt point has been cleared. This method is necessary to allow several interrupts to be serviced with a single handler, if so desired.

Interrupt Example

The following example outlines the steps taken to initialize the board to cause interrupts.

1. Clear the global interrupt enable bit in the "Status/Control Resister".
2. Write the interrupt level into the "Interrupt Level Register".
3. Write vector(s) into the "Vector Registers".
4. Write proper patterns to establish the interrupt level into the Interrupt Input Polarity Register".
5. Write all 1's into the "Interrupt Clear Register " to reset interrupt inputs.
6. Write 1's into the "Interrupt Enable Register" to enable individual interrupts.
7. Write a 1 into the global interrupt enable bit of the "Status/Control Register".

Interrupts may now occur from the board.

When the board asserts an interrupt, the following action takes place:

1. The host processor asserts IACK* and a level of the interrupt it is seeking, and if the level matches the board's, the board puts a vector out on the data bus lines D0-D7. The original interrupt request from the board remains asserted.
2. The host processor uses the vector to determine the software interrupt handler to execute, and then executes it. For a single handler per point scheme, the handler writes to the proper bit in the "Interrupt Clear" register to remove the interrupt request. This also clears its interrupt pending flag and interrupt input flag. If other points have interrupts pending, another interrupt request is asserted (or just remains) and upon returning from the handler, another interrupt cycle is started.
3. If a software handler is used to handle several points, it could service them at the same time that it services the original interrupt by examining the "Interrupt Pending Register" to determine what other interrupts need servicing.

Service of Interrupts

The following examples outline the steps necessary to service an interrupt from the AVME948x.

<u>Example A:</u>

1. Disable the interrupt point(s) by writing a "zero" to the individual bit(s) in the Interrupt Enable Register.
2. Clear the interrupt point(s) by writing a "one" to the individual bit(s) in the Interrupt Pending/Clear Register.
3. Then reenable the interrupt point(s) by writing a "one" to the individual bit(s) in the Interrupt Enable Register.

<u>Example B:</u>

1. Clear the Global Interrupt Enable bit in the Status Register.
2. Clear the Interrupt point(s) by writing a "one" to the individual bit(s) in the Interrupt Pending/Clear Register.
3. Then reenable the Global Interrupt Enable bit in the Status Register.

The interrupt input stimulus must be removed before the interrupt can be cleared.

4.0 THEORY OF OPERATION

This section provides a functional description of the AVME948x Digital I/O Board which consists of the following functional blocks:

- VME address decode
- VME control logic
- Digital I/O map decode logic
- Identification PROM
- Status register
- VME interrupter
- Input comparators/buffers
- Output latches/drivers

A block diagram is shown in Drawing 4500-741. Refer to the Schematic and Parts Location Drawing 4500-737 for the items referenced in the following information.

VMEbus INTERFACE

The VMEbus Interface logic contains the logic necessary to interface the Digital I/O points to the VMEbus. This logic includes VME address decode logic, the VME Control logic and the VME Interrupter logic.

The VME Address Logic

The Digital I/O Board interfaces with the VMEbus as a non-intelligent slave in the short I/O address space. The card will recognize two of the Address Modifer Codes, the Short Supervisory Access (2DH), and the Short Non-Supervisory Access (29H) codes. Jumper J19 selects the Address Modifer Code that the card will recognize. The starting address of the Digital I/O Board is determined by jumpers on pins 1-12 of J17. This allows the Digital I/O Board to reside in any one of the 64, 1K blocks of the short I/O address space.

Integrated circuit U55 compares the VME address lines (A10 - A15) and the Address Modifier line (AM2) to Jumpers J17 and J19. If the two are equal, then the EQ* line is asserted. U57 checks the remaining Address Modifier Lines and AS*, and then asserts the CDEN* (card enable) line.

The VME Control Logic

The VME control logic takes care of the Data Transfer Acknowledge (DTACK*) timing and the Bus Error (BERR*) logic. The Digital I/O Board will assert the VME BERR* signal if the host CPU tries to access the card using a long-word read or write data transfer. U57 and U43 control the DTACK* timing. The transfer ackowledge delay signal (DDLAY) is asserted when the card has been properly decoded and either of the data strobes (DS1*, DS0*) are asserted. This allows U43 to start shifting a logical "1" across its outputs. The delay time is programmed by the factory through jumper J18. When DTACK is asserted, it is inverted through U42 and the VME DTACK* signal is asserted.

The VME Interrupter

The VME interrupter block diagram is shown in Drawing 4500-740. Refer to the schematic and parts location Drawing 4500-737 for the items referenced in the following paragraphs.

The VME interrupter on the Digital I/O card is a Release on Register Access (RORA) type interrupter and will return an eight bit vector during the interrupt acknowledge cycle. The RORA type interrupter will release the interrupt request line (IRQx*) after the interrupt has been cleared. The interrupter logic contains a programmable interrupt level accessible through the Interrupt Level Register.

The eight I/O interrupt points are level sensitive and work on a first come, first serve basis, unless the interrupts occur at the same time. If two or more interrupts occur at the same time, then I/O interrupt point 7 has the highest priority with I/O interrupt point 0 having the lowest priority. Each I/O interrupting point may be programmed with its own interrupt vector. Also, each I/O interrupt point may be individually masked, and the polarity may be selected. The Interrupt Vector Register is contained in U30. U15 is the Interrupt Enable Register. The Enable Register is read through U9 and U10. U28 is the Interrupt Polarity Register.

When the I/O interrupt inputs sense the proper level on one of the I/O interrupt points of Port 0 the interrupter logic will assert the pre-programmed interrupt request level (IRQ7* - IRQ1*) and then monitor the Interrupt Acknowledge Input (IACKIN*) line. When the IACKIN* is asserted, the logic compares the VME address lines A1, A2, and A3 to the pre-programmed interrupt level. If the lines are not equal, it will pass the signal along by asserting IACKOUT*. If the lines are equal, it will then drive the data bus with the vector associated with the I/O interrupting point and assert the DTACK* signal. U53 controls the interrupt request level decoding. U61 contains the Interrupt Level Register and controls all VME interrupt interface signals. U25 senses an incoming interrupt request from the I/O interrupt point(s), enables U53, selects the proper address for the interrupt vector RAM, and will give priority to simultaneous interrupt requests. The Interrupt Pending Register is U11 and U12. The Interrupt Inputs Register is contained in U26 and U27. Both the Interrupt Pending and Interrupt Inputs Register are read through U13 and U14.

DIGITAL I/O PORT REGISTERS (READ/WRITE)

The I/O Port Registers reflect and/or control the state of the bidirectional I/O points. Points are grouped eight to a port. To use a point as an input, first write a "0" to it to cause the open-collector output driver to go into an OFF (high impedance) state. That lets the point be pulled to a high voltage level by an onboard pull-up resistor. The point may then be driven by an external device. Reading the point will reflect the INVERTED level at the I/O connector.

To use a point as an output, write "1" or "0" to the point as desired. If the point is read, it will reflect the state of the output as well. Note that because inverted logic is used, a high level at the I/O connector is read as "0" in the port register, and a low level is read as a "1". This is consistent with the use of open-collector outputs to drive relays and switches. A logic "1" in the computer produces a low level at the output driver to "pull in" a relay or turn something "on".

Input Comparators/Buffers

Analog voltage comparators are used as input devices to allow the inputs to withstand up to 30V (see Drawing 4500-742). During normal operation, REF is held at +5V which establishes a reference voltage of approximately 1.8 volts from voltage divider R23 & R24, which appears at the inverting inputs of all the comparators for that group. Resistors R21 and R22 along with comparator U8 form a hysteresis switch with a lower threshold of 1V and an upper threshold of 2.2V. Buffer U38 is used to put the comparator outputs for the port on the data bus during read operations.

Output Latches/Drivers
(Refer to Drawing 4500-742 for the following discussion)

Output latch/driver U52 contains 8 CMOS latches and 8 open-collector darlington transistors. Removable resistor network R57 provides pullup for the I/O lines and is usually pulled up to +5V on the card through jumper J7. Each output has a protection diode, Dp which is usually tied to the relay supply voltage when driving relay coils. This diode clamps the high voltage spike (reverse emf) that can occur when a relay coil is turned off quickly.

5.0 SERVICE AND REPAIR INFORMATION

This section provides calibration procedures, service diagrams and instructions on how to obtain service and repair assistance.

SERVICE AND REPAIR ASSISTANCE

It is highly recommended that a non-functioning board be returned to Acromag for repair. Acromag uses tested and burned-in parts, and in some cases, parts that have been selected for characteristics beyond that specified by the manufacturer. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is fully tested, placed in a burn-in room at elevated temperature, and then retested before shipment. Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before attempting calibration or repair, be sure that all of the procedures in Section 2 (Preparation For Use) have been followed. These procedures are necessary since the board has jumpers that must be properly configured.

Note: It has been observed that on occassion, a "boot" program for a disk operating system will "hang" waiting for the VMEbus SYSFAIL* signal to be released by an intelligent disk controller board. Acromag's non-intelligent slave boards assert the SYSFAIL* signal as described to the VMEbus Specification, and therefore, the disk operating system will remain "hung". The best solution to this problem is to correct the boot program so that it is no longer dependent upon the SYSFAIL* signal. When this solution is not practical, it is possible to disconnect the SYSFAIL* from the circuitry on the Acromag board by removing the jumper for J20.

CALIBRATION PROCEDURE

Due to the digital nature of the AVME948x, no maintenance is required during normal operation of the board.

REPLACEABLE PARTS

The Replaceable Parts List (Table 5.1) is provided as an aid to the user in troubleshooting the board. Replacement parts and repair services are available from Acromag. If repair is deemed necessary for this circuitry, it is highly recommended that the board be returned to Acromag for repair and recalibration. Information on ordering replacement parts is shown below:

Table 5.1: AVME 948x Replacement Parts

REFERENCE	ACROMAG PART NO.	DESCRIPTION
U1-8,16-23	1033-152	IC LM339
U9,10,13,14,40	1033-278	IC SN74LS257AND
U11,12	1033-256	IC SN74LS08ND
U15,28	1033-275	IC SN74LS273ND
U24,29	1033-273	IC SN74LS244ND
U25	5016-073	IC PA7024
U26	5016-074	IC PLS153N
U27	5016-075	IC PLS153N
U30	1033-415	IC LH5116-15
U31-38	1033-272	IC SN74LS240ND
U39	5016-076	IC PLS153N
U41	1033-621	IC N74F04N
U42	1033-623	IC N74F38N
U43	1033-658	IC 74LS164N
U44, (9480)	5016-078	IC TBP18S030N3
U44, (9481)	5016-079	IC TBP18S030N3
U45-52	1033-515	IC UCN5801ABU
U53	1033-048	IC 7445
U54	5016-082	IC PLS173N
U55	1033-626	IC AM25LS2521PCB
U56	1033-283	IC SN74LS373ND
U57	5016-083	IC PLS173N
U58	5016-077	IC PLS153N
U59,60	1033-627	IC SN74LS645-1ND
U61	5016-084	IC PAL22V10

6.0 SPECIFICATIONS

The following specifications apply at 25°C ambient temperature and nominal power supply values, unless otherwise noted.

AMBIENT TEMPERATURE RANGES

Operating Temperature............. 0 to +70°C
Storage Temperature................ -25 to +85°C

PHYSICAL DIMENSIONS

Length.. 233mm
Width... 160mm
Board Thickness........................ 1.6mm
Maximum Component Height..... 13.9mm

CONNECTORS

P1, P2....................................... IEC Type 603-2-C096MX-XXX or equivalent.
P3, P4....................................... 50-Pin Header Connector, Right Angle Amp 1-499919-0 or equivalent.

POWER REQUIREMENTS

+5 Volts DC............................. 4.875 to 5.25V DC at 1.6A, Typical (Board Logic only). Does not include additional current for output loads.

VMEbus Loading Current	Input LOW	Input HIGH
AM2, AS*, IACK*	-0.6 mA	20 uA
A15 - A10	-0.4 mA	20 uA
AM5 - AM3, AM1, AM0, LWORD*, A9 - A6, IACKIN*	-0.25 mA	25 uA
A5 - A1, DS1*, DS0*, WRITE*	-0.2 mA	20 uA
D15 - D0	-0.1 mA	20 uA
SYSRESET*	-100 uA	40 uA

VMEbus Drive Current	Output LOW	Output HIGH
IRQ7* - IRQ1*	80mA	250uA
DTACK*, BERR*, SYSFAIL*	64mA	-3.0mA
D15-D0	48mA	-15mA
IACKOUT*	24mA	-3.2mA
Typical VMEbus Access Time[1]	< 590nS[1] typical	

Note 1: Measured from the falling edge of DSx*, to the falling edge of DTACK*, during a normal data transfer cycle.

MAXIMUM INPUT FREQUENCY

Minimum positive pulse width.... 1.4 uS
Minimum negative pulse width... 2.0 uS
Maximum input frequency (w/ minimum pulse widths)........ 295 KHz
Maximum input frequency (with 50% duty cycle)................ 250 KHz

DIGITAL INPUT/OUTPUT NON-ISOLATED

Input Voltage Range.................. 0.0 to 30V DC
Input Threshold (L to H)............ 2.2V DC Nominal (Adjustable)
Input Threshold (H to L)............ 1.0V DC Nominal (Adjustable)
Input Hysteresis........................ 1.2 V DC Nominal
Input Current (pull-up resistors removed)........ 61uA at 30VDC
Points per Board........................ 64 I/O points (Each point can be configured as an input or output. Up to eight points can interrupt the VME bus)
Output Type.............................. Open collector with optional pull-up resistor.
Output Voltage Range................ 0 to 30 V DC.
Output Current Sink.................. 100mA Max.
Output Saturation Voltage.......... 1.1V Max @100mA., 0.9V Typ
Logic Compatibility.................... TTL, LSTTL, CMOS, & Others
Minimum interrupt point pulse width to guarantee recognition... >2uS

VME COMPLIANCE

Meets or exceeds all written VME Specifications per revision C.1 dated October, 1985, and IEC 821-1987

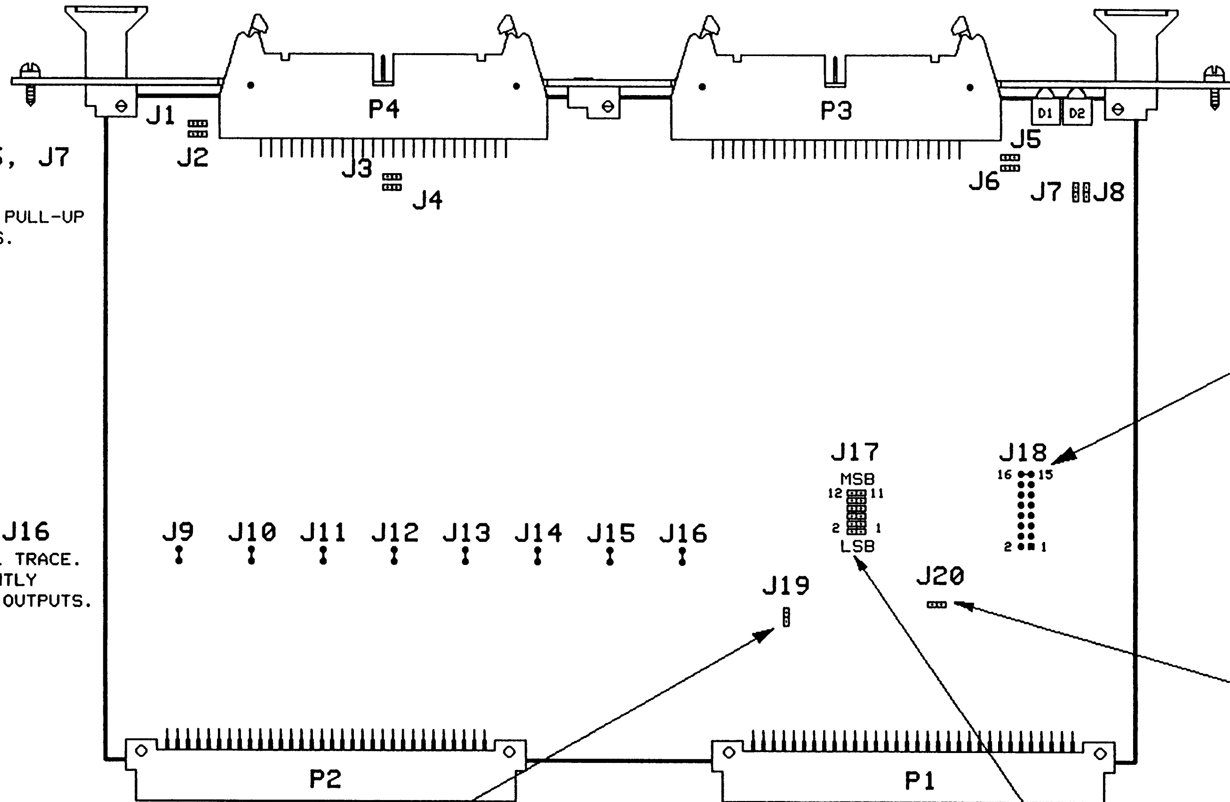
Data transfer bus........................ A16: D16/D08 (EO) DTB slave
Address modifier codes.............. 29H, 2DH
Interrupt request levels............... IRQ(1) - IRQ(7), eight programmable vectors
Memory map.............................. Short I/O space user or supervisor & occupying 1Kbyte consecutive locations, base address jumper-configurable within 64K short I/O space
Board Size................................. Double Eurocard (NEXP) (233mm X 160mm)

JUMPERS J1, J3, J5, J7
RESISTOR PULLUP JUMPER

JUMPER INSTALLED CONNECTS PULL-UP RESISTOR PACKS TO +5 VOLTS.

JUMPERS J2, J4, J6, J8
INPUT REFERENCE JUMPER

JUMPER INSTALLED CONNECTS REFERENCE TO +5 VOLTS.



JUMPERS J9 THRU J16
FACTORY INSTALLED BY FOIL TRACE. CUTTING A JUMPER PERMANENTLY DISABLES THAT GROUP OF 8 OUTPUTS.

J18
FACTORY INSTALLED. DO NOT CHANGE, POSITION CAN VARY.

VME BUS SYSFAIL JUMPER
J20 SYSFAIL JUMPER
FACTORY INSTALLED
BOARD WILL ASSERT SYSFAIL AFTER POWER UP OR RESET.

J19

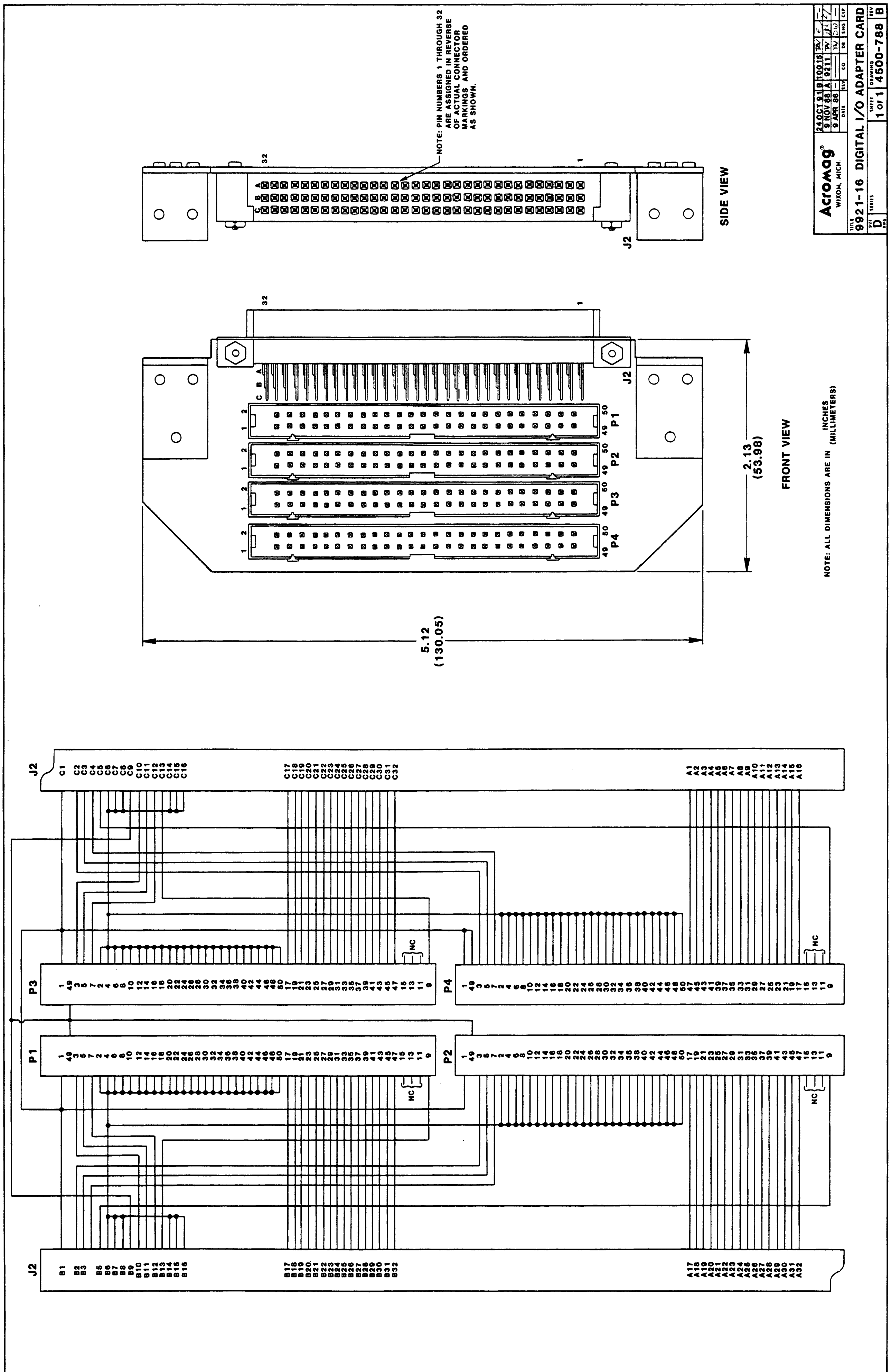
JUMPER INSTALLED - BOARD WILL RECOGNIZE BOTH SUPERVISORY AND NON-PRIVELEDGED

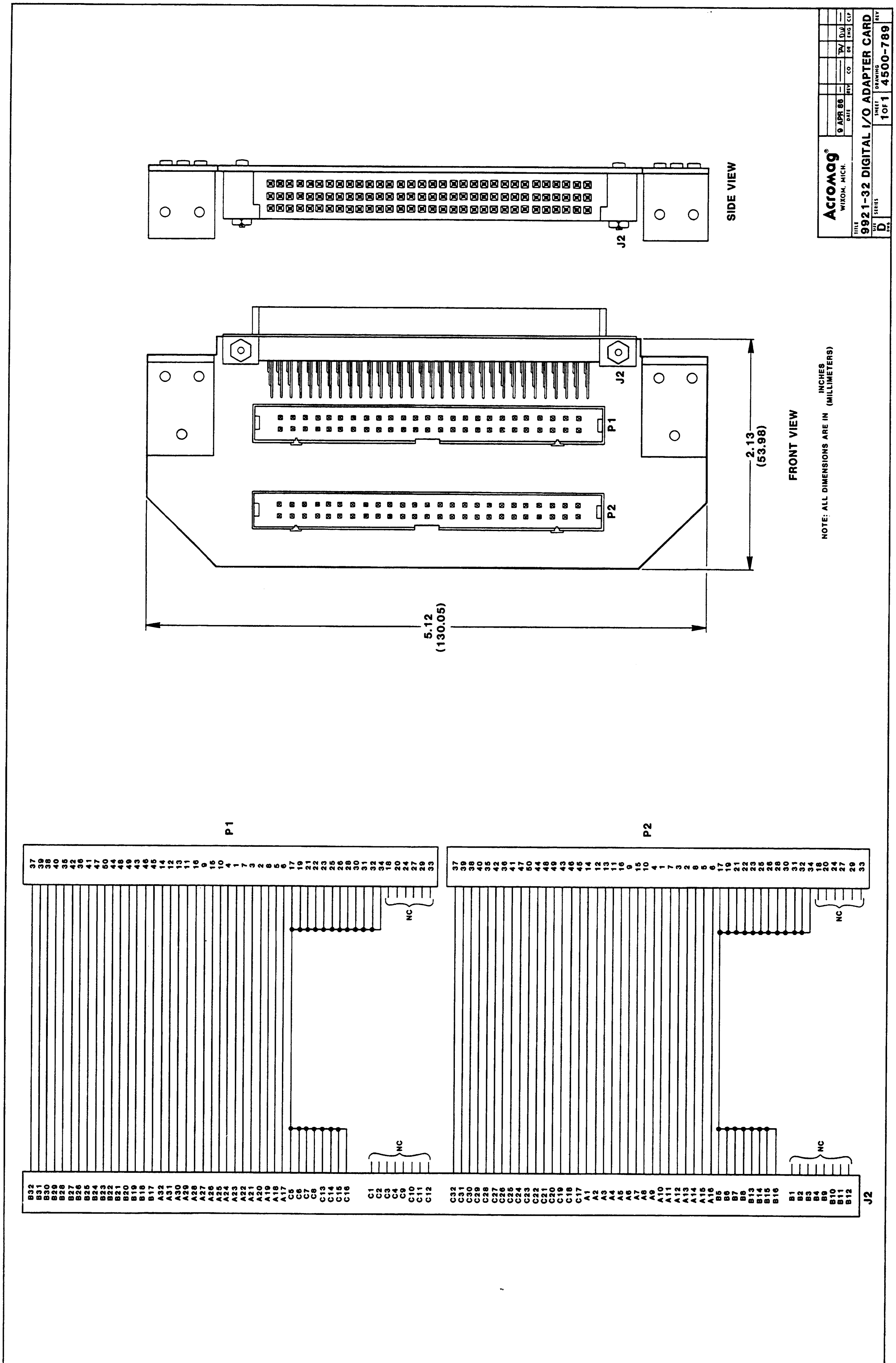
NO JUMPER INSTALLED - BOARD WILL RECOGNIZE SUPERVISORY ONLY

J17 VME BUS ADDRESS DECODING JUMPER

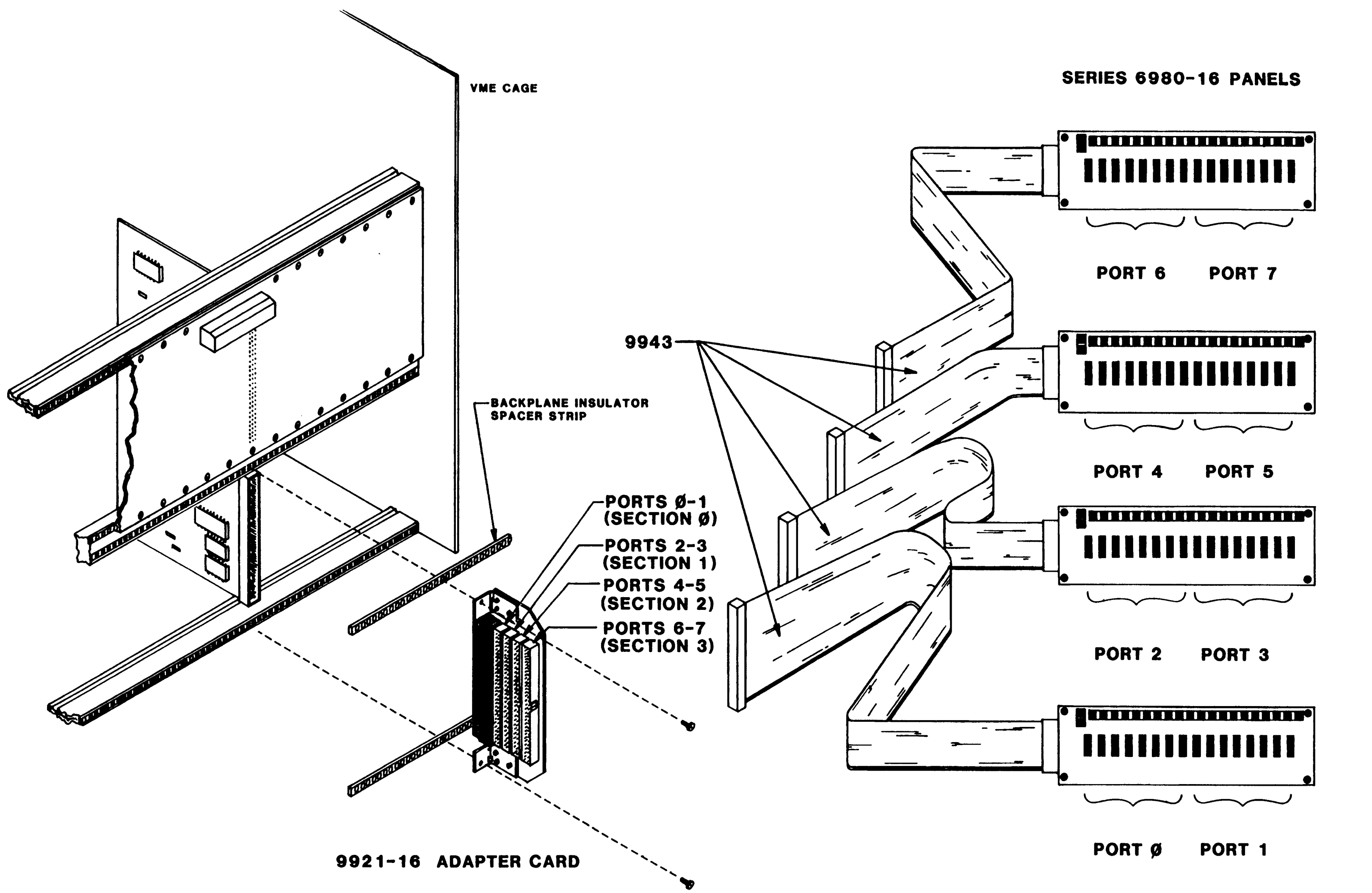
BASE ADDRESS	PINS ON J17 11 & 12	10 & 9	8 & 7	6 & 5	4 & 3	2 & 1
0000H	OUT	OUT	OUT	OUT	OUT	OUT
0400H	OUT	OUT	OUT	OUT	OUT	IN
0800H	OUT	OUT	OUT	OUT	IN	OUT
F400H	IN	IN	IN	IN	OUT	IN
F800H	IN	IN	IN	IN	IN	OUT
FC00H	IN	IN	IN	IN	IN	IN

AcroMag® WIXOM, MICH.	26 MAR 97 B 97C009 TAV GRL GRL	22 AUG 89 A 9436 TAV DK RD	11 JULY 89 - ——— SK DK —	DATE RV CO DR ENG CLP
TITLE JUMPER LOCATION				
SIZE D DWG	SERIES AVME 948X	SHEET 1 OF 1	DRAWING 4500-981	REV B


NOTE: PIN NUMBERS 1 THROUGH 32 ARE ASSIGNED IN REVERSE OF ACTUAL CONNECTOR MARKINGS AND ORDERED AS SHOWN.
SIDE VIEW
FRONT VIEW
2.13
(53.98)
5.12
(130.05)
NOTE: ALL DIMENSIONS ARE IN INCHES (MILLIMETERS)
P1
P2
P3
P4
J2
Acromag
WIXOM, MICH.
9921-16 DIGITAL I/O ADAPTER CARD
4500-788
B



SIDE VIEW
J2
FRONT VIEW
P1
P2
2.13
(53.98)
5.12
(130.05)
NOTE: ALL DIMENSIONS ARE IN INCHES (MILLIMETERS)
NC
Acromag
WIXOM, MICH.
9 APR 86
9921-32 DIGITAL I/O ADAPTER CARD
1 OF 1
4500-789
D



9921-16 ADAPTER CARD

NOTE: 9921-16 ADAPTER CARD IS NOT P2 SAFE.

DO NOT PLUG THIS ADAPTER CARD INTO
ANY P2 BACKPLANES IN A VME CAGE

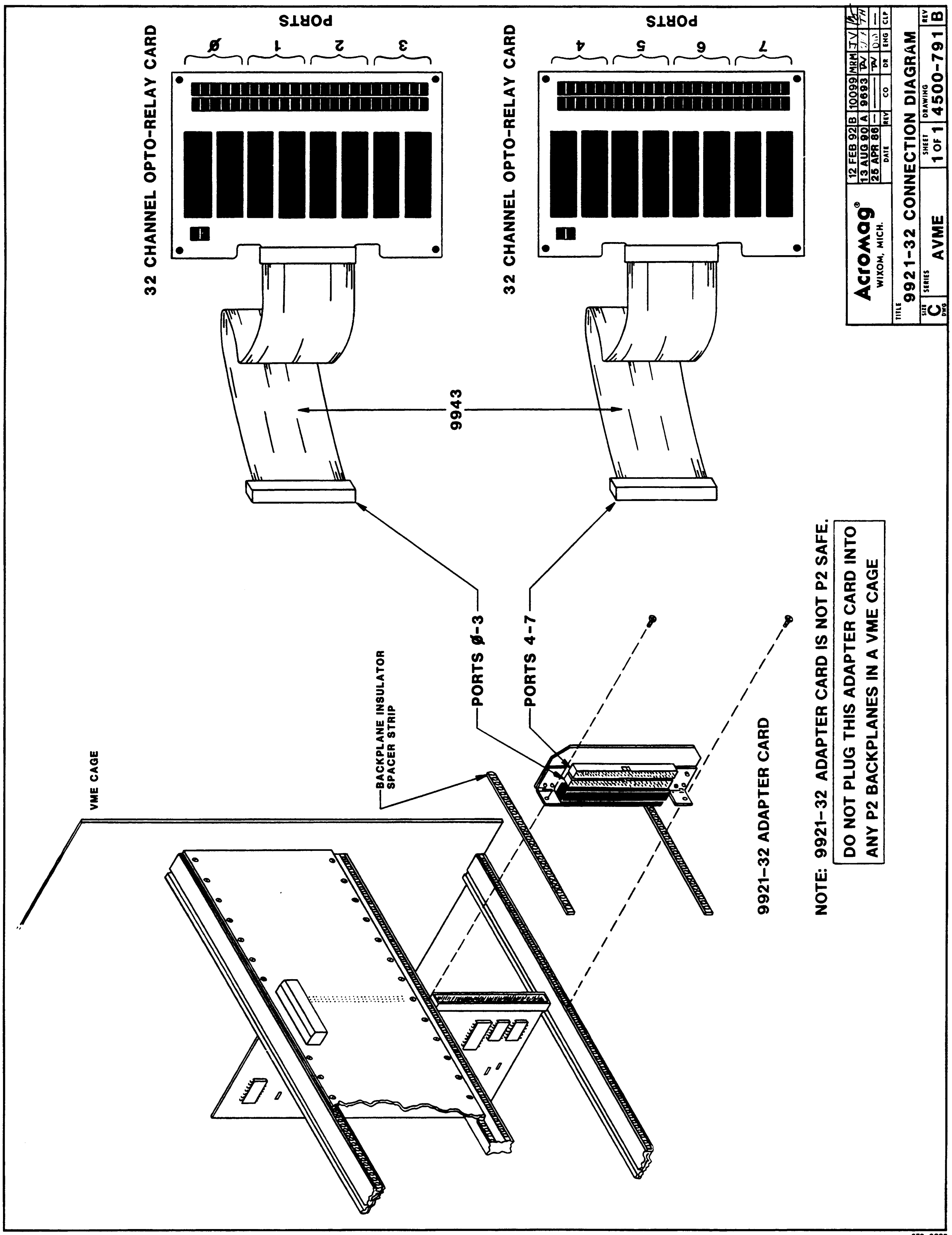
DATE	REV	CO	DR	ENG	CLP
12 FEB 92	C	10099	MRM	JV	
24 OCT 91	B	10015			TH
13 AUG 90	A	9693			TH
18 APR 86	—	——	SJK	DW.	—

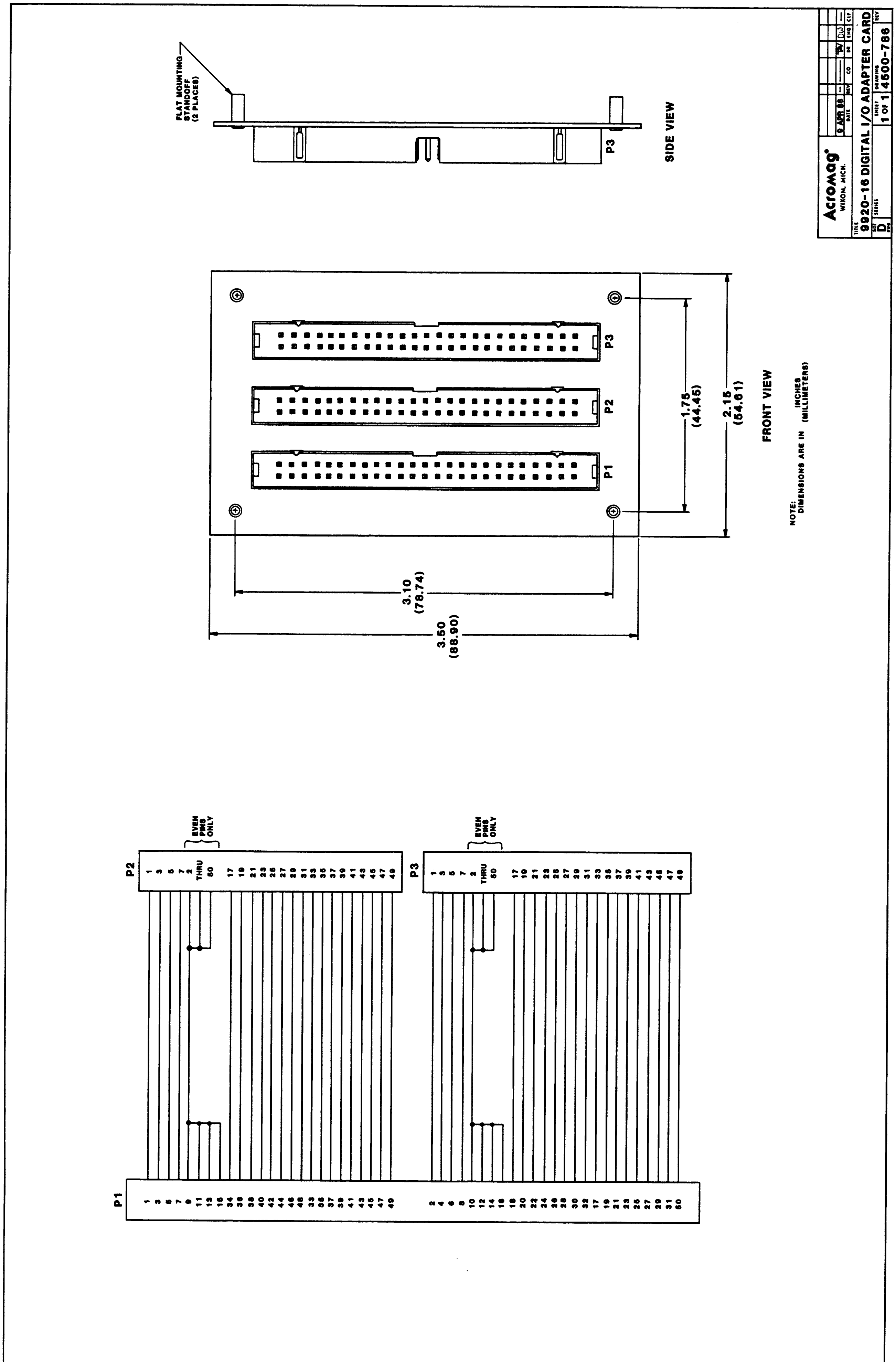
Acromag® WIXOM, MICH.

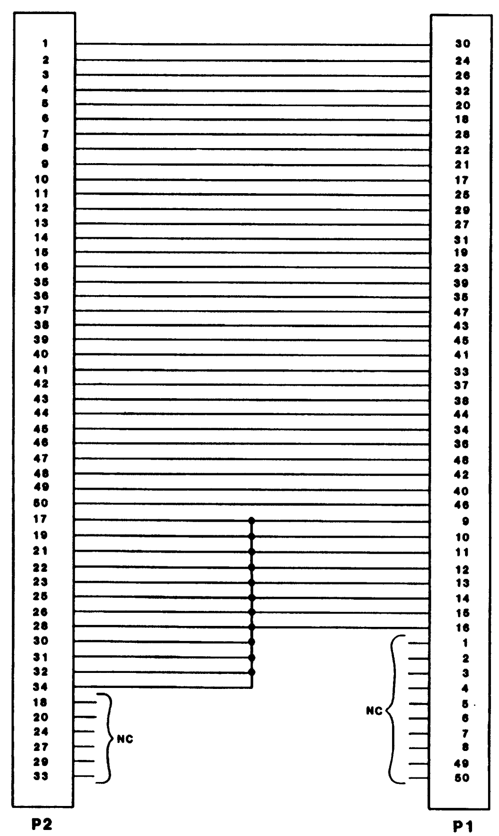
TITLE 9921-16 CONNECTION DIAGRAM

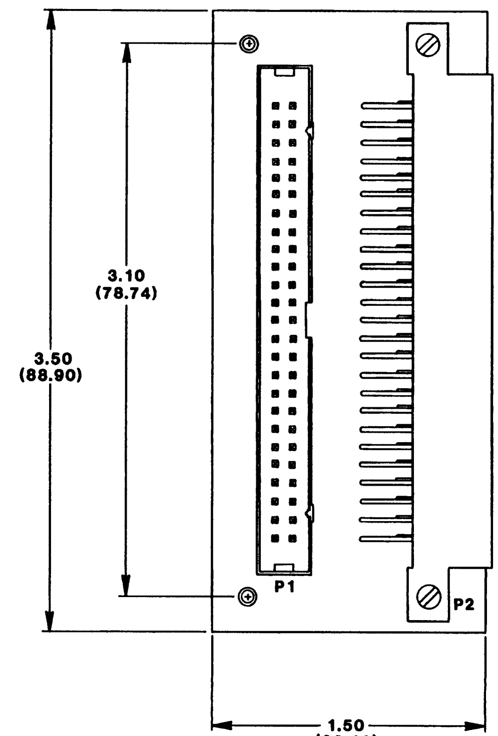
SIZE DWG	SERIES	SHEET	DRAWING	REV
C	AVME	1 OF 1	4500-790	C

3600-025

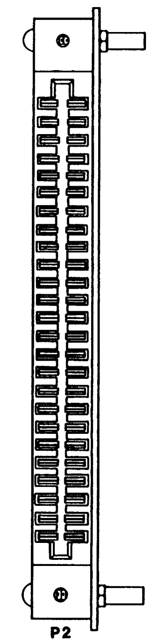

32 CHANNEL OPTO-RELAY CARD
PORTS
Ø
1
2
3
32 CHANNEL OPTO-RELAY CARD
PORTS
4
5
6
7
9943
PORTS Ø-3
PORTS 4-7
VME CAGE
BACKPLANE INSULATOR SPACER STRIP
9921-32 ADAPTER CARD
NOTE: 9921-32 ADAPTER CARD IS NOT P2 SAFE.
DO NOT PLUG THIS ADAPTER CARD INTO ANY P2 BACKPLANES IN A VME CAGE
Acromag®
WIXOM, MICH.
12 FEB 92 B 10099 MRM
13 AUG 90 A 9693
25 APR 86
DATE REV CO DR ENG CLP
TITLE 9921-32 CONNECTION DIAGRAM
SIZE C
SERIES AVME
SHEET 1 OF 1
DRAWING 4500-791
REV B
3600-025


FLAT MOUNTING STANDOFF (2 PLACES)
P3
SIDE VIEW
P3
P2
P1
1.75 (44.45)
2.15 (54.61)
FRONT VIEW
NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS)
3.10 (78.74)
3.50 (88.90)
Acromag
WIXOM, MICH.
9 APR 86
9920-16 DIGITAL I/O ADAPTER CARD
D
1 OF 1
4500-786
EVEN PINS ONLY
THRU
50
P2
P3
P1





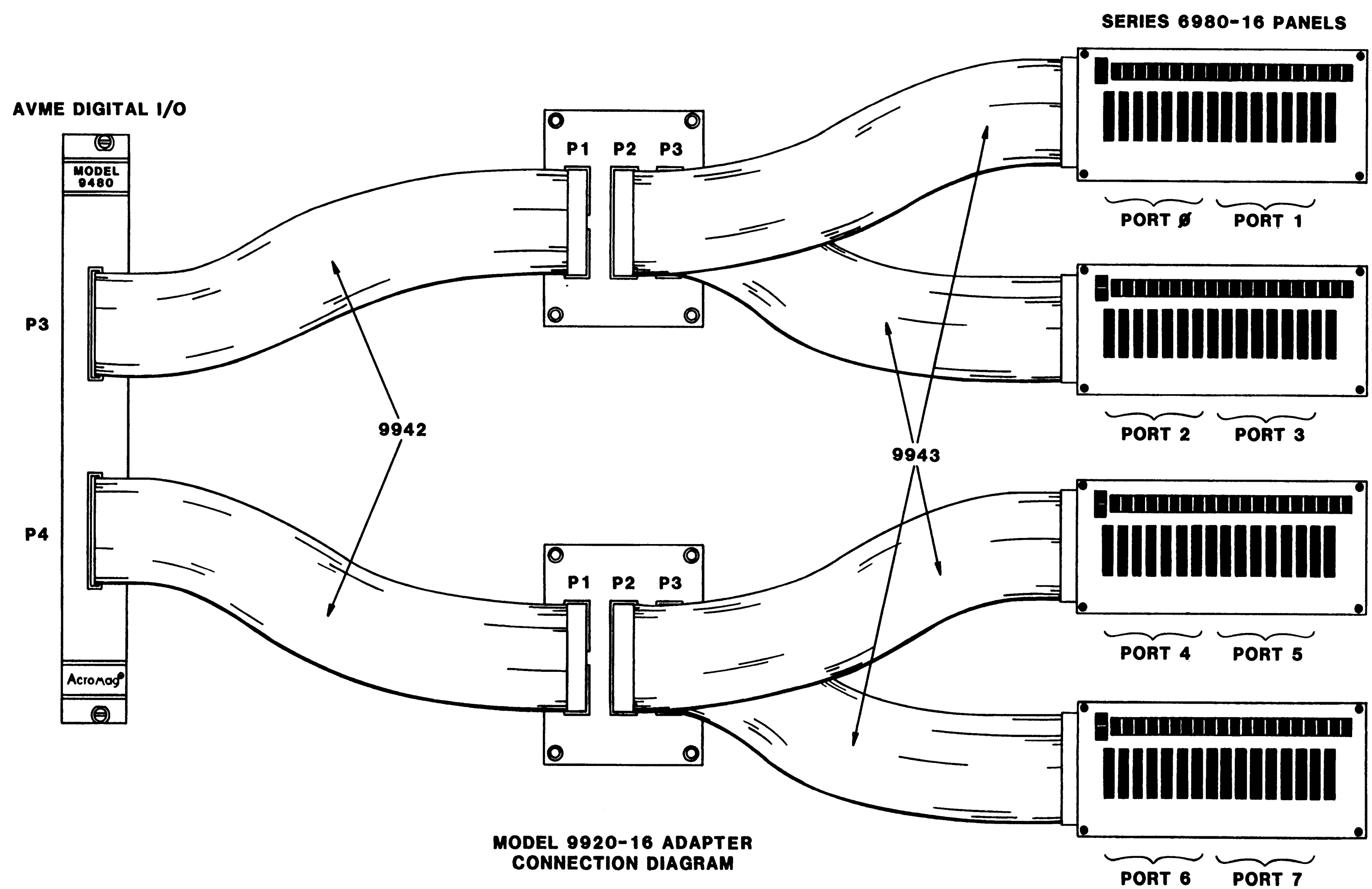
FRONT VIEW



SIDE VIEW

NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS)

Acromag® WIXOM, MICH.	9 APR 86	—	——	TV	DW	
	DATE	REV	CO	DR	ENG	CLP
TITLE 9920-32 DIGITAL I/O ADAPTER CARD						
SIZE D DWG	SERIES	SHEET 1 OF 1	DRAWING 4500-787			REV



MODEL 9920-16 ADAPTER
CONNECTION DIAGRAM

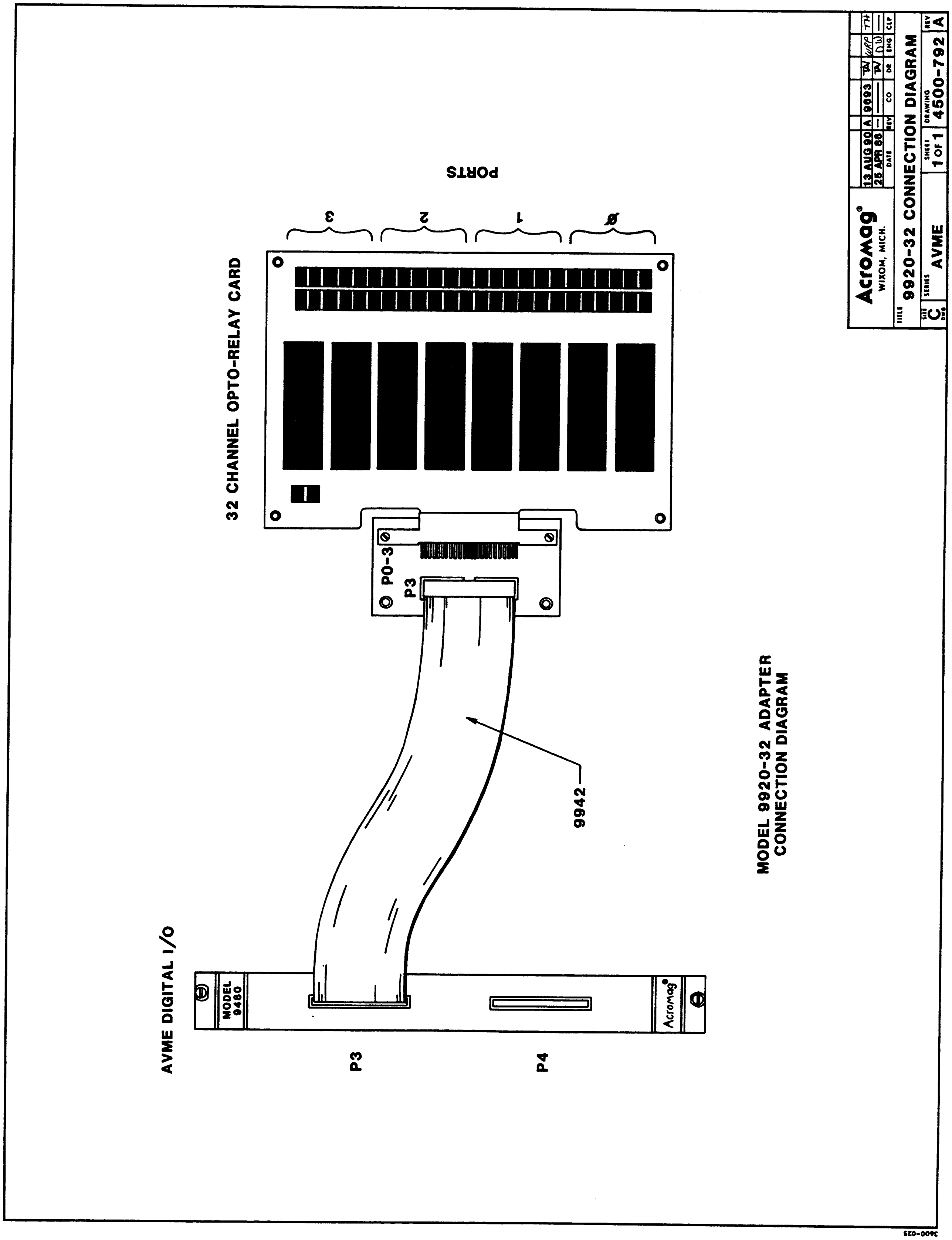
13 AUG 90	B	9693	TAV	WRP	TH
2 JUNE 87	A	8773	SJK	DS	KD
7 APR 86	—	——	TAV	DW	—
DATE	REV	CO	DR	ENG	CLP

Acromag® WIXOM, MICH.

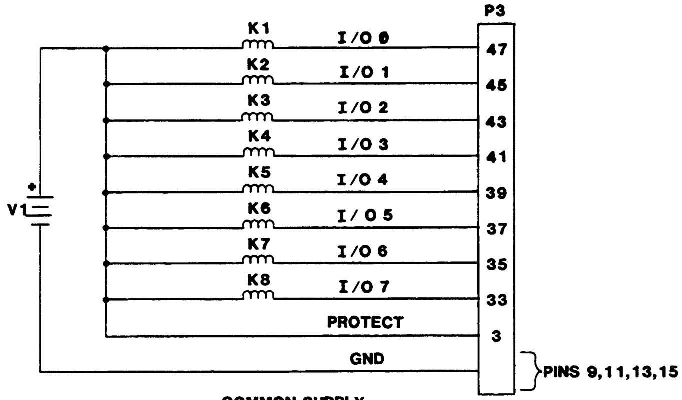
TITLE 9920-16 CONNECTION DIAGRAM

SIZE DWG C | SERIES | SHEET 1 OF 1 | DRAWING 4500-785 | REV B

3400-025


32 CHANNEL OPTO-RELAY CARD
PORTS
3
2
1
Ø
P0-3
P3
9942
MODEL 9920-32 ADAPTER
CONNECTION DIAGRAM
AVME DIGITAL I/O
MODEL 9480
Acromag
P3
P4
Acromag
WIXOM, MICH.
13 AUG 90 A 9693
25 APR 86 —
DATE REV CO DR ENG CLP
TITLE 9920-32 CONNECTION DIAGRAM
SIZE C
SERIES AVME
SHEET 1 OF 1
DRAWING 4500-792
REV A
3400-025

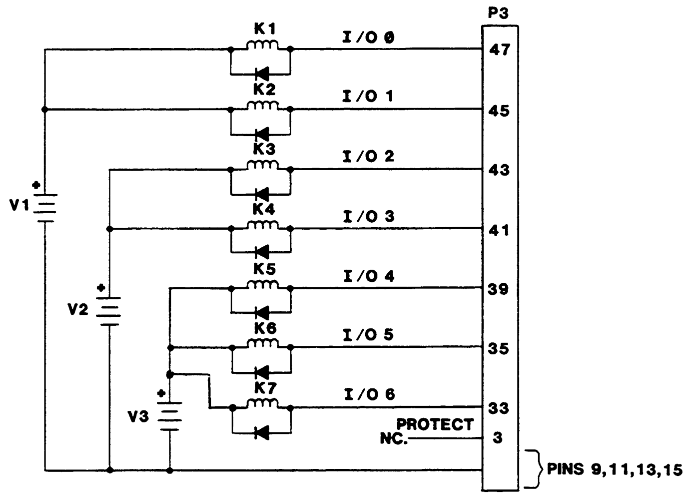
Acromag®
WIXOM, MICH.
RELAY DRIVER & INPUT CONFIGURATIONS
D AVME 948X 4500-743 C



COMMON SUPPLY-

PROTECT LINE TIED TO V1,
PUTS A PROTECTION DIODE
ACROSS EACH RELAY.

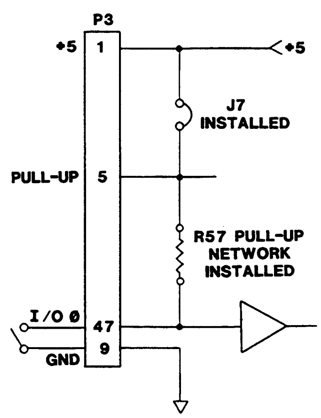
NOTE: PULL-UPS
ON AVME-9480
SHOULD BE REMOVED.



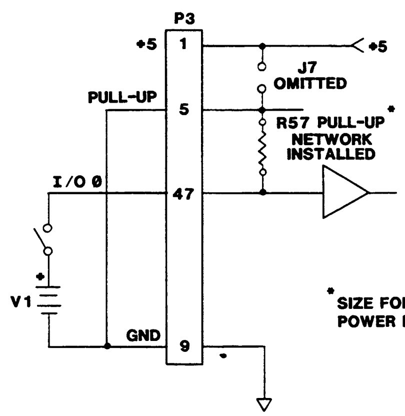
SEPARATE SUPPLIES-

EACH RELAY NEEDS ITS
OWN EXTERNAL DIODE.

RELAY DRIVER CONFIGURATIONS
(SHOWN FOR PORTS N & 0)



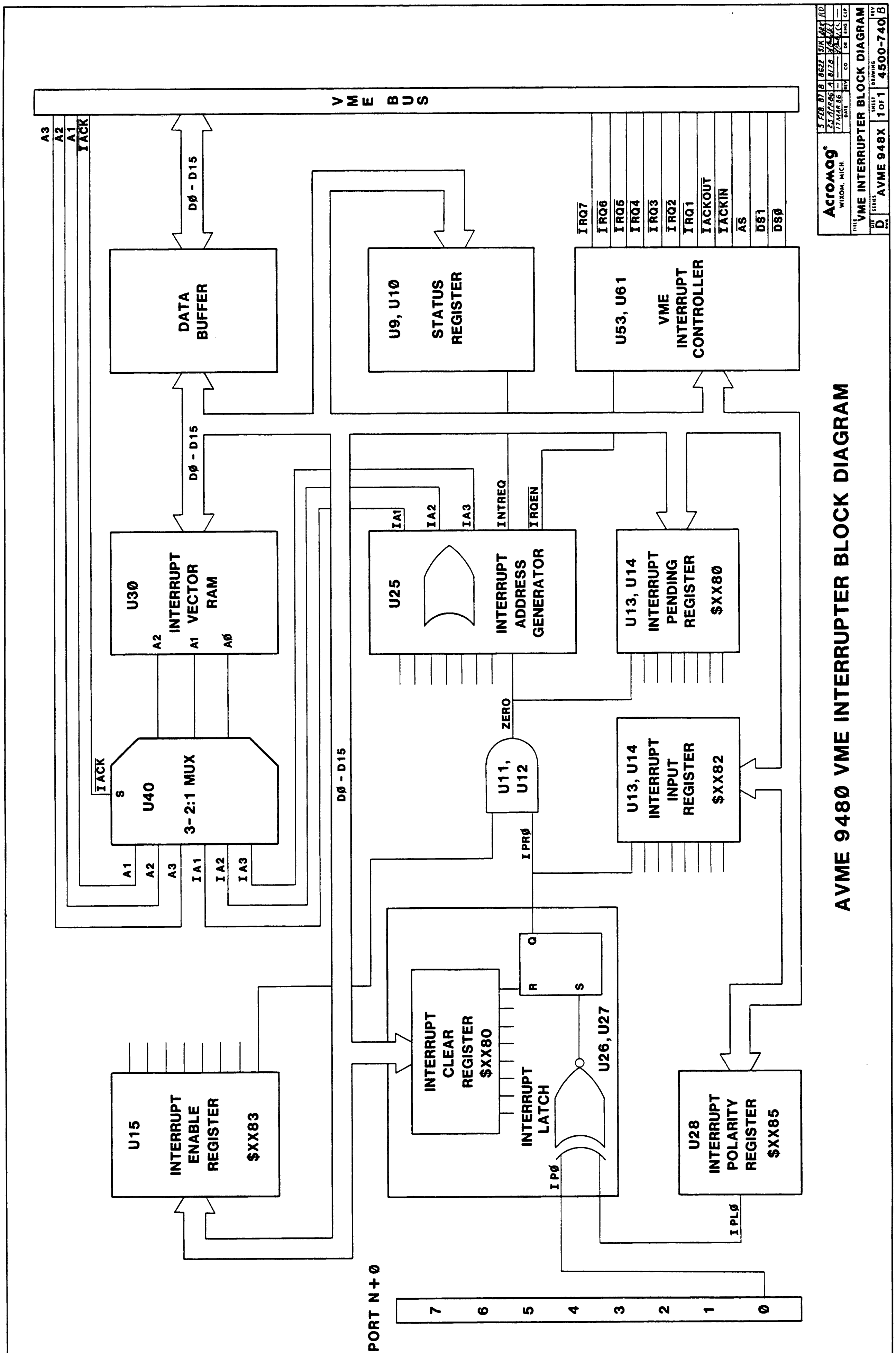
SIMPLE CONTACT CLOSURE SENSING.



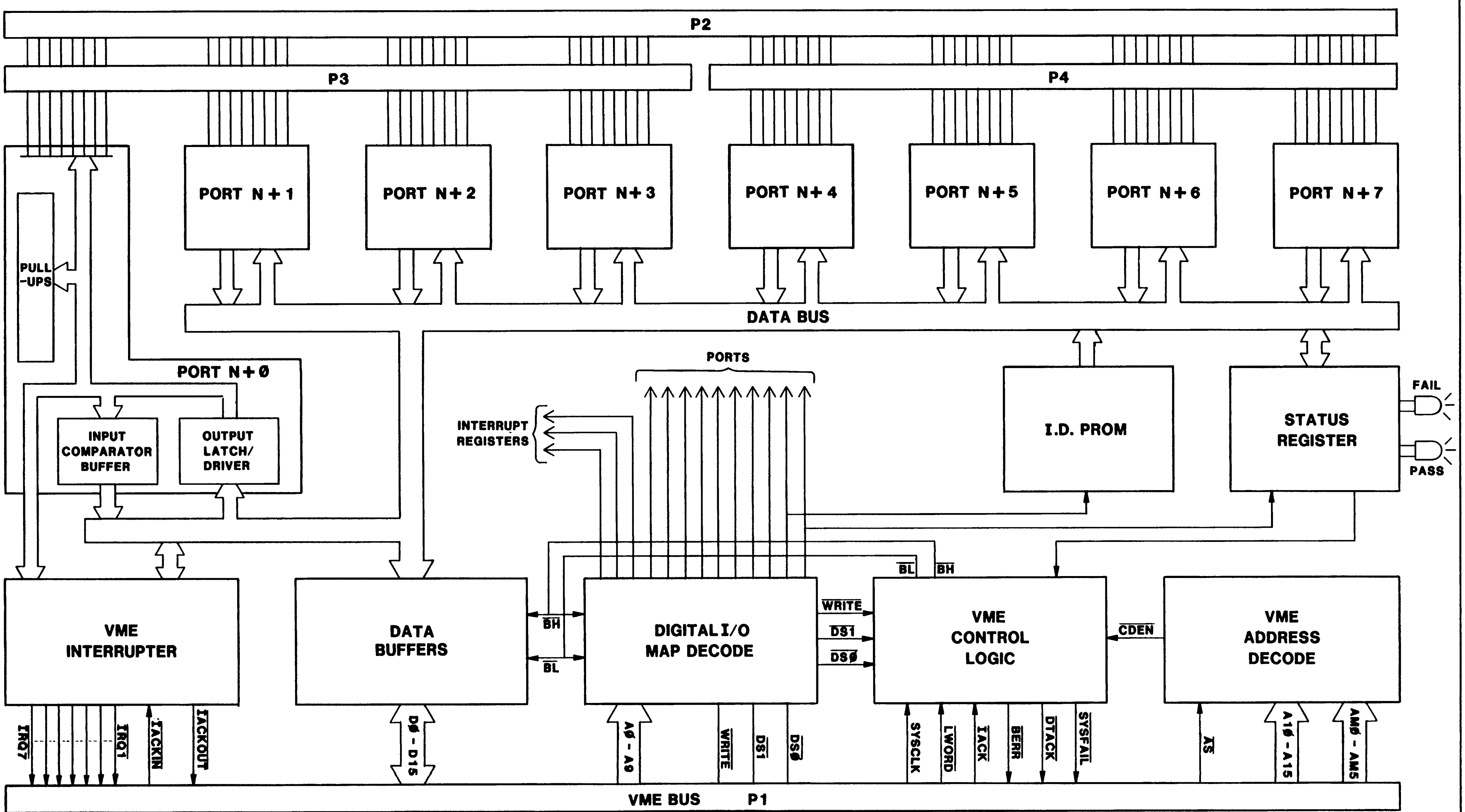
*SIZE FOR PROPER
POWER DISSIPATION

CONTACTS SWITCHING A VOLTAGE.

INPUT CONFIGURATIONS
(SHOWN FOR PORTS N & 0, I/O POINT 0)

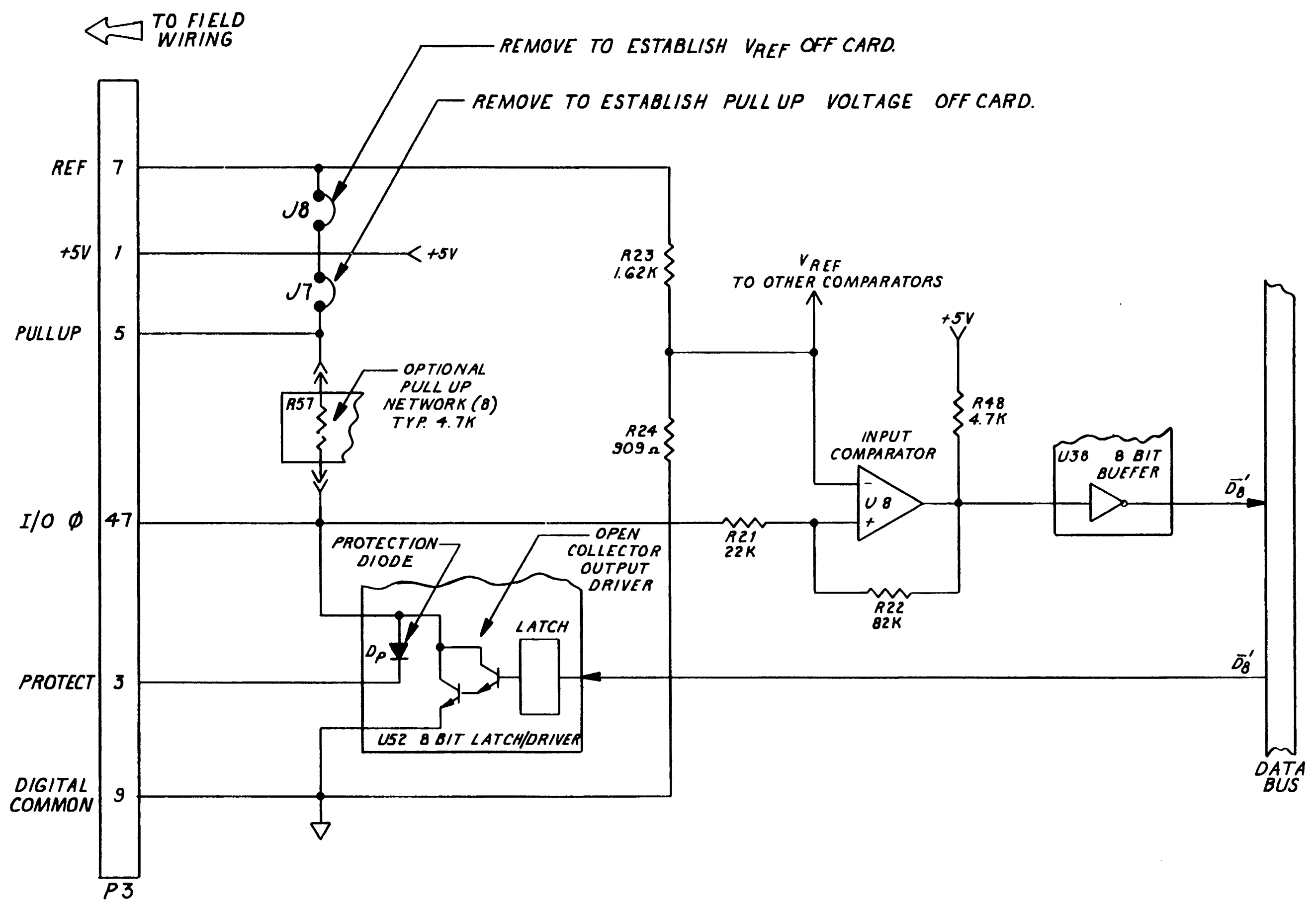


AVME 9480 VME INTERRUPTER BLOCK DIAGRAM



AVME 9480 BLOCK DIAGRAM

Acromag WIXOM, MICH.	23 APR 86 A 8173 / 14 MAR 86 —
TITLE	AVME 9480 BLOCK DIAGRAM
SIZE D	SERIES 948X · SHEET 1 OF 1 · DRAWING 4500-741 · REV A



SIMPLIFIED I/O POINT SCHEMATIC
(1 OF 8 PER PORT)

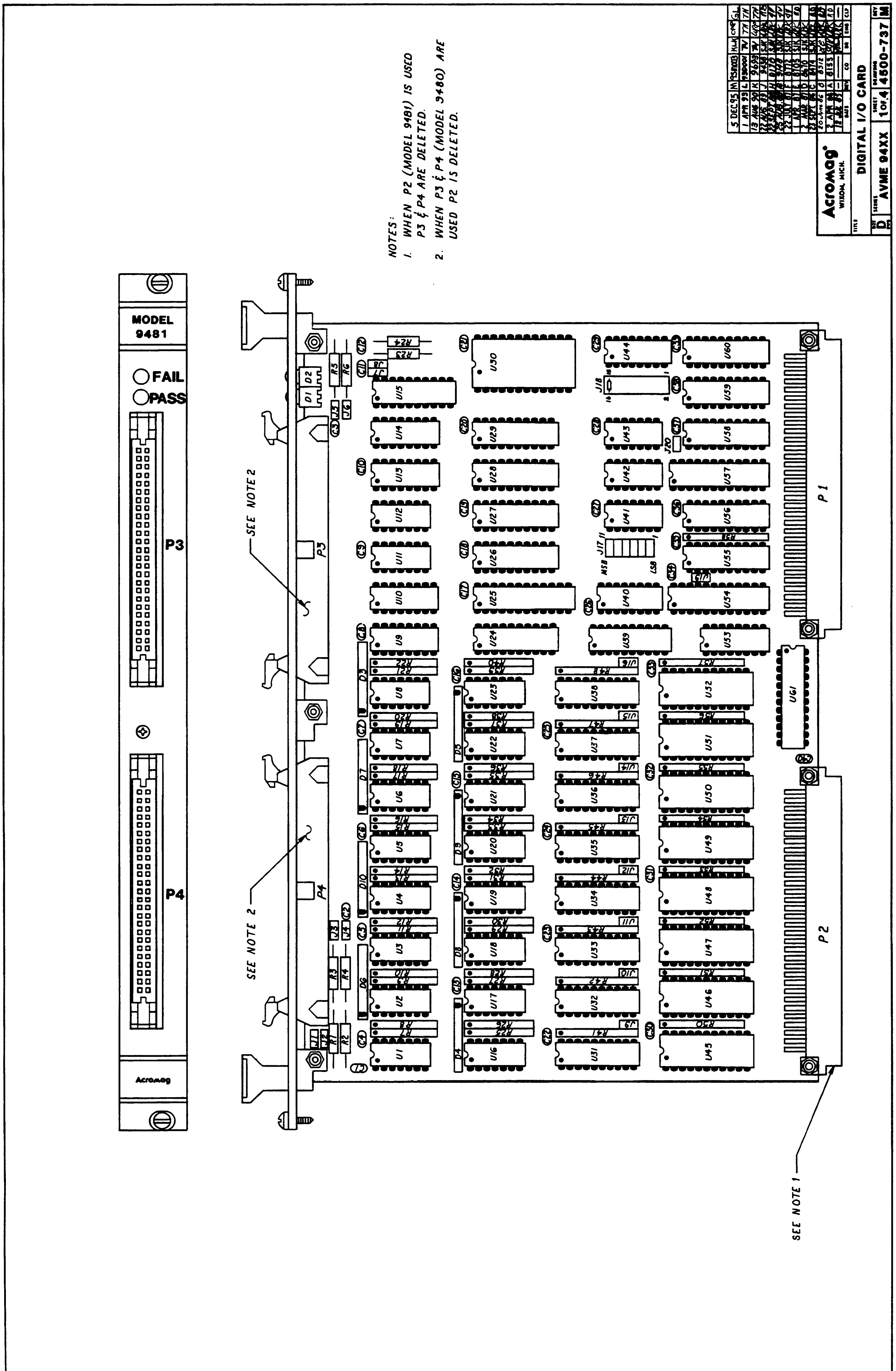
DATE	REV	CO	DR	ENG	CLP
5 FEB 87	B	8621	SJK		RD
23 APR 86	A	8180			
17 MAR 86	—	—			—

Acromag® WIXOM, MICH.

TITLE AVME 9480 SIMPLIFIED SCHEMATIC

SIZE C DWG | SERIES 948X | SHEET 1 OF 1 | DRAWING 4500-742 | REV B

3600-025


NOTES:
1. WHEN P2 (MODEL 9481) IS USED P3 & P4 ARE DELETED.
2. WHEN P3 & P4 (MODEL 9480) ARE USED P2 IS DELETED.
MODEL 9481
FAIL
PASS
P3
P4
Acromag
SEE NOTE 2
SEE NOTE 1
P1
P2
Acromag
WIXOM, MICH.
DIGITAL I/O CARD
D
AVME 94XX
1 OF 4
4500-737
M